## CLAIMS

What is claimed is:

1. An apparatus, comprising:

a seed register within an integrated circuit to receive a seed vector;

a linear feedback shift register within the integrated circuit to provide a bit pattern using the seed vector; and

a signature register within the integrated circuit to provide a compressed response at a conclusion of a test of the integrated circuit, wherein the seed register, the linear feedback shift register, and the signature register each have a register length such that the register lengths of the seed register, the linear feedback shift register, and the single input signature register are equal.

2. The apparatus of claim 1, wherein the linear feedback shift register and the signature register each have a shift frequency such that the shift frequencies of the linear feedback shift register and the signature register are equal and greater than a frequency at which the seed vector is loaded into the seed register.

3. The apparatus of claim 1, wherein the signature register is a single input signature register.

4. The apparatus of claim 1, further including a test controller within the integrated circuit to provide the seed vector to the seed register, to provide bits to the linear feedback shift register, and to receive the compressed response from the signature register.

5. An apparatus, comprising:

a seed register within an integrated circuit to receive a seed vector;

a linear feedback shift register within the integrated circuit to provide a bit pattern using the seed vector;

a signature register within the integrated circuit to provide a compressed response at a conclusion of a test of at least a portion of the integrated circuit, wherein the seed register, the linear feedback shift register, and the signature register each have a register length such that the register lengths of the seed register, the linear feedback shift register, and the single input signature register are equal; and

a number of scan chains, each scan chain having an initial scan cell and a final scan cell, wherein the initial scan cell of each scan chain is populated through the linear feedback shift register and the test response is compacted into the signature register from the final scan cells of the number of scan chains.

6. The apparatus of claim 5, wherein the number of scan chains is M, where M is a positive integer, the linear feedback shift register has a register length of n bit cells, where n is a positive integer, n being less than M, such that an internal shift frequency for the M scan chains is greater than M/n times a frequency at which the test vector is loaded into the seed register.

7. The apparatus of claim 5, further including a number of exclusive-or logic units and a flush control input to selectively provide bits to the linear feedback shift register to control a degree to which a vector in the linear feedback shift register is dependent on previous vectors, wherein each exclusive-or logic unit is associated with one bit cell of the linear feedback shift register as an input to the associated bit cell.

8. The apparatus of claim 5, further including masking logic to provide one or more mask bits to regulate an input to the signature register.

9. The apparatus of claim 5, further including a shift control to select a horizontal mode shift or a vertical mode shift of the scan chains.

10. The apparatus of claim 5, further including a number of scan channels within an integrated circuit to receive test vectors.

11. The apparatus of claim 10, wherein the linear feedback shift register has a shift frequency to shift out a test vector at a rate M times faster than a rate at a seed vector is loaded into the seed register, M being the number of scan channels.

12. The apparatus of claim 10, wherein the number of scan chains is divided into a number of groups of scan chains, and the linear feedback shift register has a number of different internal taps to substantially load each group of scan chains simultaneously.

13. The apparatus of claim 12, further including a phase shifter to load bits into each group of the group of scan chains from the linear feedback shift register.

14. The apparatus of claim 12, wherein the signature register is a multiple input signature register having an input from each group of the group of scan chains.

15. A method of testing comprising:

loading a seed register in an integrated circuit with a seed vector;

transferring the seed vector in the seed register to a linear feedback shift register;

generating bit patterns using the linear feedback shift register to load a slice of a scan load of a scan chain; and

compacting a response into a signature register from a scan slice at a final scan cell bit position of a scan chain.

16. The method of claim 15, wherein the method further includes using the feedback shift register to generate bits patterns and compacting a response into a signature register for a first seed vector in parallel with loading a second seed vector into seed register.

17. The method of claim 15, wherein compacting a response into a signature register includes compacting a response into a single input signature register.

18. The method of claim 15, wherein compacting a response into a signature register includes compacting a response into a multiple input signature register.

19. The method of claim 15, wherein the method further includes shifting scan cells of a number of scan chains loaded through the linear feedback shift register at a shift frequency that is greater than a ratio of the number of scan chains to a register length of the linear feedback shift register times a frequency for loading a seed vector into the seed register.

20. The method of claim 15, wherein the method further includes masking one or more bits being input into the signature register.

21. The method of claim 15, wherein the method further includes selectively providing bits to the linear feedback shift register to control a degree to which a vector in the linear feedback shift register is dependent on previous vectors.

22. A system comprising:

a scan based integrated circuit; and

an electronic device coupled to the scan based integrated circuit, wherein the scan based integrated circuit includes:

a seed register within an integrated circuit to receive a seed vector;

a linear feedback shift register within the integrated circuit to provide a bit pattern using the seed vector;

a signature register within the integrated circuit to provide a compressed response at a conclusion of a test of at least a portion of the integrated circuit, wherein the seed register, the linear feedback shift register, and the signature register each have a register length such that the

register lengths of the seed register, the linear feedback shift register, and the single input signature register are equal; and

a number of scan chains, each scan chain having an initial scan cell and a final scan cell, wherein the initial scan cell of each scan chain is populated through the linear feedback shift register and the test response is compacted into the signature register from the final scan cells of the number of scan chains.

23. The system of claim 22, wherein the linear feedback shift register and the signature register each have a shift frequency such that the shift frequencies of the linear feedback shift register and the signature register are equal and greater than a frequency at which the seed vector is loaded into the seed register.

24. The system of claim 22, wherein the signature register is a single input signature register.

25. The system of claim 22, further including a number of exclusive-or logic units and a flush control input to selectively provide bits to the linear feedback shift register to control a degree to which a vector in the linear feedback shift register is dependent on previous vectors, wherein each exclusive-or logic unit is associated with one bit cell of the linear feedback shift register as an input to the associated bit cell.

26. The system of claim 22, further including a shift control to select a horizontal mode shift or a vertical mode shift of the scan chains.

27. The system of claim 22 further including a number of scan channels within the integrated circuit to receive test vectors, wherein the number of scan chains is divided into a number of groups of scan chains, the linear feedback shift register has a number of different internal taps to substantially load each group of scan chains

simultaneously, and the signature register is a multiple input signature register having an input from each group of the group of scan chains.

28. The system of claim 22, wherein the scan based integrated circuit is a processor and the electronic device is a memory device.

29. The system of claim 22, wherein the scan based integrated circuit is an ASIC integrated circuit.

30. The system of claim 22, wherein the electronic device is a tester external to the scan based integrated circuit.